

## **SSC8640GN4**

### N and P-Channel Enhancement Mode Power MOSFET

#### Features

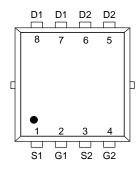
#### **N-Channel**

V <sub>DS</sub>	$V_{GS}$	R <sub>DS(ON)</sub> Typ.	Ι <sub>D</sub>
40V	±20V	15mΩ@10V	28A
700	V	20mΩ@4V5	20/1

#### **P-Channel**

V <sub>DS</sub>	V <sub>GS</sub>	R <sub>DS(ON)</sub> Typ.	I <sub>D</sub>
-40V	±20V	26mΩ@-10V	-21A
-40 V	<u> </u>	34mΩ@-4V5	-217

## Pin configuration



PDFN3.3X3.3-8L (Top View)

## Description

The SSC8640GN4 uses advanced trench technology to provide excellent RDS(ON) and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

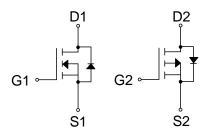
## 100% UIS + $\Delta VDS$ + Rg Tested!

## Applications

- PWM Applications
- Load Switch
- DC-DC Converters

# Ordering Information

Device	Package	Shipping	
SSC8640GN4	PDFN3.3X3.3-8L	5000/Reel	



Pin Configuration



**Marking** 

(YW: Internal Traceability Code)



## ➤ Absolute Maximum Ratings (T<sub>A</sub>=25°C unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-to-Source Voltage		V <sub>DSS</sub>	40	-40	V
Gate-to-Source Voltage		V <sub>GSS</sub>	±20	±20	V
Cantinua Drain Current	T <sub>A</sub> = 25°C		28	-21	Α
Continuous Drain Current a	T <sub>A</sub> = 100°C	l <sub>D</sub>	15	-11	Α
Pulsed Drain Current b		Ірм	110	-84	Α
Power Dissipation <sup>a</sup>		IDSM	9	-7	Α
Dawar Dissination C	T <sub>A</sub> = 25°C	Б	19	19	W
Power Dissipation °	T <sub>A</sub> = 100°C	P <sub>D</sub>	7	7	W
Operation junction temperature		TJ	-55 to 150	-55 to 150	$^{\circ}$
Storage temperature range		Тѕтс	-55 to 150	-55 to 150	$^{\circ}$

### ➤ Thermal Resistance Ratings (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Rati	Unit		
Symbol	Faranietei	N-Channel	P-Channel	Offic	
Reja	Junction-to-Ambient Thermal Resistance a	55	55	°C // //	
Rejc	Junction-to-Case Thermal Resistance	6.5	6.5	°C/W	

#### Note:

- a. The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper,in a still air environment with  $T_A$ =25 °C. The value in any given application depends on the user is specific board design. The current rating is based on the t≤10s thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation  $P_D$  is based on  $T_{J(MAX)}$ =150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

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# ➤ N-Channel Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250µA	40			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250uA$	1	1.5	2	V
Drain Course On Registeres		V <sub>GS</sub> = 10V, I <sub>D</sub> = 8A		15	21	0
Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 4A		20	29	mΩ
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V			-1	μA
Gate-Source Leak Current	Igss	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA
Transconductance	G <sub>FS</sub>	$V_{DS} = 5V$ , $I_D = 5A$		35		S
Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = 8A		0.8	1.3	V
Input Capacitance	Ciss	V 00V V 0V		870		
Output Capacitance	Coss	$V_{DS} = 20V$ , $V_{GS} = 0V$ , $f = 1MHz$		67		рF
Reverse Transfer Capacitance	C <sub>RSS</sub>	I = IIVIMZ		8		
Total Gate Charge	Q <sub>G</sub>	V 40V.V 00V		27		
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 20V,		3.1		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 10A		6.2		
Turn-on Delay Time	T <sub>D(ON)</sub>			6		
Rise Time	Tr	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 20V, R <sub>L</sub>		11		
Turn-off Delay Time	T <sub>D(OFF)</sub>	= $10\Omega$ , $R_{GEN} = 6\Omega$		24		ns
Fall Time	Tf			9.8		



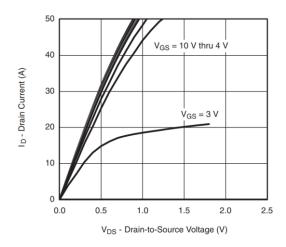


# > P-Channel Electrical Characteristics (T<sub>A</sub>=25℃ unless otherwise noted)

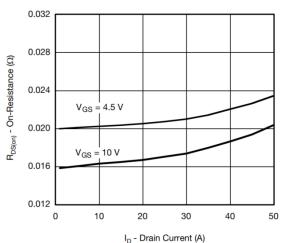
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-40			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250uA$	-1	-1.5	-2	V
Drain Course On Registeres	_	$V_{GS} = -10V, I_D = -7A$		26	45	0
Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4A		34	55	mΩ
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = -40V, V <sub>GS</sub> = 0V			-1	μA
Gate-Source Leak Current	Igss	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±100	nA
Transconductance	G <sub>FS</sub>	V <sub>DS</sub> = -5V, I <sub>D</sub> = -5A		20		s
Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = -7A		-0.8	-1.3	V
Input Capacitance	Ciss	V 20V V 0V		1300		
Output Capacitance	Coss	$V_{DS} = -20V$ , $V_{GS} = 0V$ , $f = 1MHz$		122		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>	T = TIVIMZ		8		
Total Gate Charge	Q <sub>G</sub>	N 001/ N 401/		23		
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = -20V, V <sub>DS</sub> = -10V,		1.9		nC
Gate to Drain Charge	$Q_{GD}$	$I_D = -7A$		4.4		
Turn-on Delay Time	T <sub>D(ON)</sub>			8		
Rise Time	Tr	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -20V,		6		
Turn-off Delay Time	T <sub>D(OFF)</sub>	$R_L = 2.9\Omega$ , $R_G = 6\Omega$ ,		21		ns
Fall Time	T <sub>f</sub>			7		



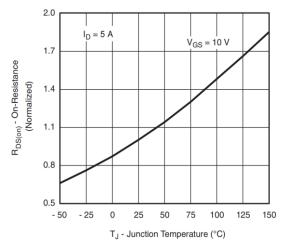
## N-Channel Typical Performance Characteristics (T<sub>A</sub>=25℃ unless otherwise noted)



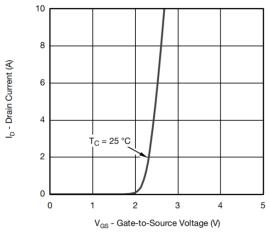
#### **Output Characteristics**



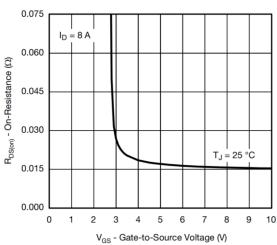
On-Resistance vs. Drain Current



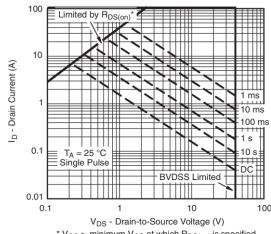
On-Resistance vs. Junction Temperature



**Transfer Characteristics** 



On-Resistance vs. Gate-to-Source Voltage

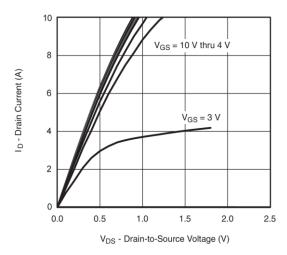


\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

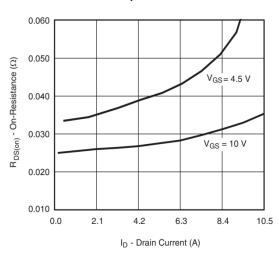
Safe Operating Area, Junction-to-Ambient



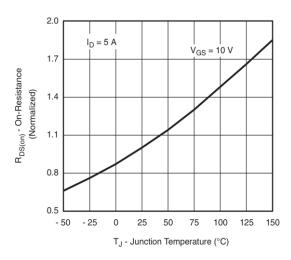
# ▶ P-Channel Typical Performance Characteristics ( $T_A$ =25 $^{\circ}$ C unless otherwise noted)



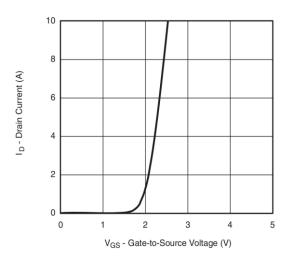
#### **Output Characteristics**



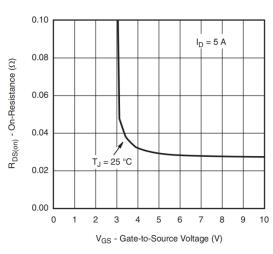
On-Resistance vs. Drain Current



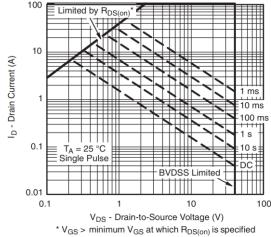
On-Resistance vs. Junction Temperature



**Transfer Characteristics** 



On-Resistance vs. Gate-to-Source Voltage

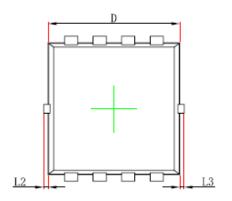


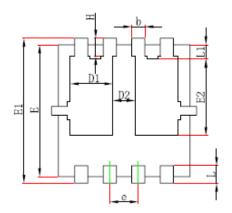
Safe Operating Area, Junction-to-Ambient

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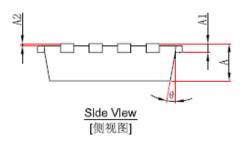
## Package Information





Top Vlew [顶视图]

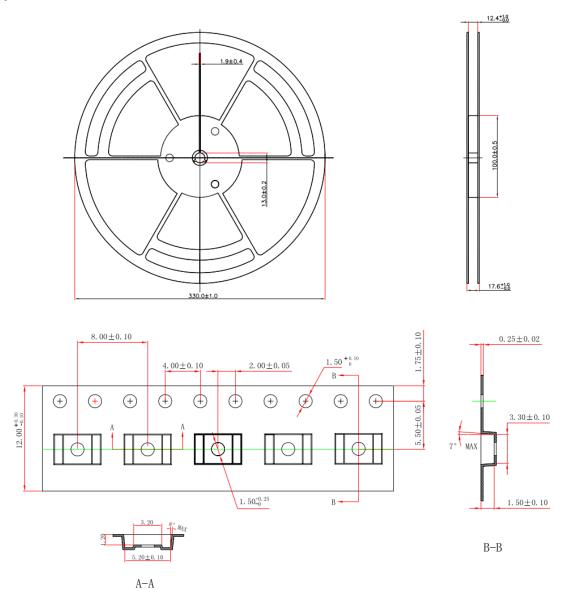
Bottom Vlew [背视图]



Cymbol	Dimensions Ir	n Millimeters	Dimension	s In Inches
Symbol	Min.	Max.	Min.	Max.
Α	0.650	0.850	0.026	0.033
A1	0.152	REF.	0.006 REF.	
A2	0~0.	05	0~0	.002
D	2.900	3.100	0.114	0.122
D1	0.935	1.135	0.037	0.045
D2	0.280	0.480	0.011	0.019
Е	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
е	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0	.004
Н	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°



# > Tape and Reel





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